Amendments to the Specification

ABSTRACT OF THE DISCLOSURE

Please replace the Abstract of the Disclosure with the following paragraph:

In a clock delay adjusting method of a semiconductor integrated circuit device, a plurality of source points for adjusting a clock delay is provided to synchronize a value of the clock delay from each of the source points of each of hierarchical blocks in a semiconductor chip to a clock input circuit operating synchronously with a clock, according to circuit design conditions of the hierarchical blocks. Area terminals are provided in the source points, respectively. A clock input terminal of the semiconductor chip and each area terminal are connected through a clock line so as to be clock distributed over a hierarchical top. A clock delay between the hierarchical blocks is adjusted.